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1 **Synthesis of fixed-structure controllers via numerical optimization**
El Ghaoui, L.; Balakrishnan, V.;
Decision and Control, 1994., Proceedings of the 33rd IEEE Conference on , Vo 3 , 14-16 Dec. 1994
Pages:2678 - 2683 vol.3

[Abstract] [PDF Full-Text (376 KB)] **IEEE CNF**

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Schiavoni, N.; Locatelli, A.;
Decision and Control, 1991., Proceedings of the 30th IEEE Conference on , 11 Dec. 1991
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[Abstract] [PDF Full-Text (140 KB)] **IEEE CNF**

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3 **Face analysis and synthesis**
Morishima, S.;
Signal Processing Magazine, IEEE , Volume: 18 , Issue: 3 , May 2001
Pages:26 - 34

[Abstract] [PDF Full-Text (724 KB)] **IEEE JNL**

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4 **Computationally efficient optimal control methods applied to power systems**
Freitas, F.D.; Simoes Costa, A.;
Power Systems, IEEE Transactions on , Volume: 14 , Issue: 3 , Aug. 1999
Pages:1036 - 1045

[Abstract] [PDF Full-Text (700 KB)] IEEE JNL

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5 **An LMI optimization approach for structured linear controllers**
Jeongheon Han; Skelton, R.E.;
Decision and Control, 2003. Proceedings. 42nd IEEE Conference on , Volume: 5 , 9-12 Dec. 2003
Pages:5143 - 5148 Vol.5

[Abstract] [PDF Full-Text (472 KB)] IEEE CNF

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6 **Face image analysis and synthesis for human-computer interaction**
Morishima, S.;
Signal Processing Proceedings, 2000. WCCC-ICSP 2000. 5th International Conference on , Volume: 2 , 21-25 Aug. 2000
Pages:1213 - 1220 vol.2

[Abstract] [PDF Full-Text (996 KB)] IEEE CNF

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7 **Robust decentralized control using an alternating projection approa**
Kan Tan; Grigoriadis, K.N.;
American Control Conference, 2000. Proceedings of the 2000 , Volume: 2 , 28 June 2000
Pages:801 - 805 vol.2

[Abstract] [PDF Full-Text (368 KB)] IEEE CNF

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8 **Realtime face analysis and synthesis using neural network**
Morishima, S.;
Neural Networks for Signal Processing X, 2000. Proceedings of the 2000 IEEE Signal Processing Society Workshop , Volume: 1 , 11-13 Dec. 2000
Pages:13 - 22 vol.1

[Abstract] [PDF Full-Text (668 KB)] IEEE CNF

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9 **Decentralized H_∞ controller design for large-scale systems: a matrix inequality approach using a homotopy method**
Ikeda, M.; Zhai, G.; Fujisaki, Y.;
Decision and Control, 1996., Proceedings of the 35th IEEE , Volume: 1 , 11-13 Dec. 1996
Pages:1 - 6 vol.1

[Abstract] [PDF Full-Text (548 KB)] IEEE CNF

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10 **Decentralized H/sub 2/ optimal control with pole regional constrain**
Lei Zuo; Nayfeh, S.A.;
American Control Conference, 2003. Proceedings of the 2003 , Volume: 6 , 4-June 2003
Pages:5341 - 5346 vol.6

[Abstract] [PDF Full-Text (442 KB)] IEEE CNF

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11 **Decentralized overlapping control of a formation of unmanned aeria vehicles**

Stipanovic, D.M.; Inalhan, G.; Teo, R.; Tomlin, C.J.;
Decision and Control, 2002, Proceedings of the 41st IEEE Conference on , Volu 3 , 10-13 Dec. 2002
Pages:2829 - 2835 vol.3

[Abstract] [PDF Full-Text (473 KB)] **IEEE CNF**

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12 **A MATLAB package for multiobjective control synthesis**
Xin Qi; Khammash, M.H.; Salapaka, M.V.;
Decision and Control, 2001. Proceedings of the 40th IEEE Conference on , Volu 4 , 4-7 Dec. 2001
Pages:3991 - 3996 vol.4

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13 **Decentralized quadratic stabilization of large-scale systems**
Guisheng Zhai; Yasuda, K.; Ikeda, M.;
Decision and Control, 1994., Proceedings of the 33rd IEEE Conference on , Vo 3 , 14-16 Dec. 1994
Pages:2337 - 2339 vol.3

[Abstract] [PDF Full-Text (212 KB)] **IEEE CNF**

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14 **On the synthesis of optimal stack filters under structural constraint**
Lin Yin;
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on , Volume: 2 , 30 May-2 June 1994
Pages:321 - 324 vol.2

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

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15 **Design of robust static output feedback for large-scale systems**
Zecevic, A.I.; Siljak, D.D.;
Automatic Control, IEEE Transactions on , Volume: 49 , Issue: 11 , Nov. 2004
Pages:2040 - 2044

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1 Transformations for the synthesis and optimization of asynchronous distributed control

Michael Theobald, Steven M. Nowick

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(166.38 KB) Additional Information: full citation, abstract, references, citings, index terms

Asynchronous design has been the focus of renewed interest. However, a key bottleneck is the lack of high-quality CAD tools for the synthesis of large-scale systems which also allow design-space exploration. This paper proposes a new synthesis method to address this issue, based on transformations.The method starts with a scheduled and resource-bounded Control-Data Flow Graph (CDFG). Global transformations are first applied to the entire CDFG, unoptimized controllers are then e ...

2 Analog synthesis & design methodology: Remembrance of circuits past: macromodeling by data mining in large analog design spaces

Hongzhou Liu, Amit Singhee, Rob A. Rutenbar, L. Richard Carley

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(583.79 KB) Additional Information: full citation, abstract, references, citings, index terms

The introduction of simulation-based analog synthesis tools creates a new challenge for analog modeling. These tools routinely visit 103 to 105 fully simulated circuit solution candidates. What might we do with all this circuit data? We show how to adapt recent ideas from large-scale data mining to build models that capture significant regions of this visited performance space, parameterized by variables manipulated by synthesis, trained by the data points visited during synthesis. Experimental ...

3 An intermediate representation for behavioral synthesis

Nikil D. Dutt, Tedd Hadley, Daniel D. Gajski

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(728.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes an intermediate representation for behavioral and structural designs that is based on annotated state tables. It facilitates user control of the synthesis process by allowing specification of partially design structures, and a mixture of behavior, structure and user specified bindings between the abstract behavior and the structure. The format's general model allows the capture of synchronous and asynchronous behavior, and permits

hierarchical descriptions with concurre ...

4 Session 6D: Analog synthesis: The sizing rules method for analog integrated circuit design

H. Graeb, S. Zizala, J. Eckmueller, K. Antreich

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(221.02 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents the *sizing rules method* for analog CMOS circuit design that consists of: first, the development of a hierarchical library of transistor pair groups as basic building blocks for analog CMOS circuits; second, the derivation of a hierarchical generic list of constraints that must be satisfied to guarantee the function of each block and its reliability with respect to physical effects; and third, the development of an automatic recognition of building blocks in a circuit s ...

5 M32: a constructive multilevel logic synthesis system

Victor N. Kravets, Karem A. Sakallah

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(534.08 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We describe a new constructive multilevel logic synthesis system that integrates the traditionally separate technology-independent and technology-dependent stages of modern synthesis tools. Dubbed M32, this system is capable of generating circuits incrementally based on both functional as well as structural considerations. This is achieved by maintaining a dynamic structural representation of the evolving implementation and by refining it through progressive introduction of gates fr ...

Keywords: congestion, global routing, quadratic placement, relaxed pins, routing models, supply-demand

6 Performance estimation of embedded software with instruction cache modeling

Yau-Tsun Steven Li, Sharad Malik, Andrew Wolfe

July 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 4 Issue 3**

Full text available: pdf(171.05 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Embedded systems generally interact in some way with the outside world. This may involve measuring sensors and controlling actuators, communicating with other systems, or interacting with users. These functions impose real-time constraints on system design. Verification of these specifications requires computing an upper bound on the worst-case execution time (WCET) of a hardware/software system. Furthermore, it is critical to derive a tight upper bound on WCET in order to make efficient u ...

7 Session 10B: VLIW exploration and deisgn synthesis: Exploring performance tradeoffs for clustered VLIW ASIPs

Margarida F. Jacome, Gustavo de Veciana, Viktor Lapinskii

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(146.77 KB) Additional Information: full citation, abstract, references, citings

VLIW ASIPs provide an attractive solution for increasingly pervasive real-time multimedia

and signal processing embedded applications. In this paper we propose an algorithm to support trade-off exploration during the early phases of the design/specialization of VLIW ASIPs with clustered datapaths. For purposes of an early exploration step, we define a parameterized *family of clustered datapaths D(m,n),* where *m* and *n* denote *interconnect capacity* and *cluster capacity ...*

8 Resynthesis of multi-level circuits under tight constraints using symbolic optimization
Victor N. Kravets, Karem A. Sakallah
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(168.30 KB) Additional Information: full citation, abstract, references, citings, index terms

We apply recently introduced constructive multi-level synthesis in the resynthesis loop targeting convergence of industrial designs. The incremental ability of the resynthesis approach allows more predictable circuit implementations while allowing their aggressive optimization. The approach is based on a very general symbolic decomposition template for logic synthesis that uses information-theoretical properties of a function to infer its decomposition patterns (rather than more conventional mea ...

9 High-quality sub-function construction in functional decomposition based on information relationship measures
L. Józwiak, A. Chojnacki
March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(240.09 KB) Additional Information: full citation, references, citings, index terms

10 H/S Embedded Systems: Retargetable static timing analysis for embedded software
Kaiyu Chen, Sharad Malik, David I. August
September 2001 **Proceedings of the 14th international symposium on Systems synthesis**

Full text available: pdf(293.24 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a novel approach for retargetable static software timing analysis. Specifically, we target the problem of determining bounds on the execution time of a program on modern processors, *and solve this problem in a retargetable software development environment.* Another contribution of this paper is the modeling of important features in contemporary architectures, such as branch prediction, predication, and instruction pre-fetching, which have great impact on system performa ...

11 Knowledge based control in micro-architecture design
F. D. Brewer, D. D. Gajski
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(869.72 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the principles and implementation of design-process control in a micro-architecture compiler. The knowledge-base relies on both local and global evaluations to determine strategies to achieve global goals and then implements those strategies by manipulating hardware allocations and search heuristics. A system overview and annotated sample run are presented.

12 Performance estimation of embedded software with instruction cache modeling
Yau-Tsun Steven Li, Sharad Malik, Andrew Wolfe

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(145.46 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Embedded systems generally interact with the outside world. Thus, some real-time constraints may be imposed on the system design. Verification of these constraints requires computing a tight upper bound on the worst case execution time (WCET) of a hardware/software system. The problem of bounding WCET is particularly difficult on modern processors, which use cache-based memory systems that vary memory access time significantly. This must be accurately modeled in order to tightly bound WCET. Exis ...

13 Performance analysis of embedded software using implicit path enumeration

Yau-Tsun Steven Li, Sharad Malik

November 1995 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 1995 workshop on Languages, compilers, & tools for real-time systems,** Volume 30 Issue 11

Full text available: pdf(987.85 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded computer systems are characterized by the presence of a processor running application specific dedicated software. A large number of these systems must satisfy real-time constraints. This paper examines the problem of determining the extreme (best and worst) case bounds on the running time of a given program on a given processor. This has several applications in the design of embedded systems with real-time constraints. An important aspect of this problem is determining which paths in t ...

14 Session 3: The synthesis of digital machines with provable epistemic properties

Stanley J. Rosenschein, Leslie Pack Kaelbling

March 1986 **Proceedings of the 1986 conference on Theoretical aspects of reasoning about knowledge**

Full text available: pdf(1.18 MB) Additional Information: full citation, abstract, references

Researchers using epistemic logic as a formal framework for studying knowledge properties of AI systems often interpret the knowledge formula K(x, φ) to mean that machine x encodes φ in its state as a syntactic formula or can derive it inferentially. By defining K(x, φ), instead, in terms of the correlation between the state of the machine and that of its environment, the formal properties of modal system S5 can be satisfied without hav ...

15 Performance analysis of embedded software using implicit path enumeration

Yau-Tsun Steven Li, Sharad Malik

January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(89.03 KB) Additional Information: full citation, references, citings, index terms

16 Floating constraints in lexical choice

Michael Elhadad, Jacques Robin, Kathleen McKeown

June 1997 **Computational Linguistics,** Volume 23 Issue 2

Full text available: pdf(3.13 MB) Publisher Site Additional Information: full citation, abstract, references, citings

Lexical choice is a computationally complex task, requiring a generation system to consider a potentially large number of mappings between concepts and words. Constraints that aid in determining which word is best come from a wide variety of sources, including syntax,

semantics, pragmatics, the lexicon, and the underlying domain. Furthermore, in some situations, different constraints come into play early on, while in others, they apply much later. This makes it difficult to determine a systemati ...

17 The generalized boundary curve — a common method for automatic nominal design centering of analog circuits

R. Schwencker, F. Schenkel, H. Graeb, K. Antreich

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(109.51 KB) Publisher Site

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18 Technical papers: requirements engineering: Detection of conflicting functional requirements in a use case-driven approach: a static analysis technique based on graph transformation

Jan Hendrik Hausmann, Reiko Heckel, Gabi Taentzer

May 2002 **Proceedings of the 24th International Conference on Software Engineering**

Full text available: pdf(1.55 MB)

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In object-oriented software development, requirements of different stakeholders are often manifested in use case models which complement the static domain model by dynamic and functional requirements. In the course of development, these requirements are analyzed and integrated to produce a consistent overall requirements specification. Iterations of the model may be triggered by conflicts between requirements of different parties.However, due to the diversity, incompleteness, and informal nature ...

Keywords: UML, graph transformation, requirements specification, unified process, use cases

19 Knowledge-based design of LANs using system entity structure concepts

Jerzy W. Rozenblit, Süleyman Sevinc, Bernard P. Zeigler

December 1986 **Proceedings of the 18th conference on Winter simulation**

Full text available: pdf(696.70 KB)

Additional Information: full citation, abstract, references, citings, index terms

The paper illustrates an application of knowledge based system design concepts to design of local area networks. A system entity structure representation of a local area network (LAN) is developed. This representation unifies a variety of possibilities for LAN design architecture. In a design session, the LAN design domain is subsequently restricted by pruning the entity structure with respect to network design objectives. A LAN model is then synthesized using a production rule scheme. The ...

20 Design process management for CAD frameworks

M. F. Jacome, S. W. Director

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(816.20 KB)

Additional Information: full citation, references, citings, index terms

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A Framework For Enforceable Specification Of Extended.. - Georgakopoulos, Hornick (1994) (Correct) (15 citations)
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ftp.gte.com/pub/dom/workflow/IJICIS.ps

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Bayesian Graphical Models - Jensen (2000) (Correct) (1 citation)
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www.cs.auc.dk/research/DSS/papers/jensen00a.ps

Genesys: An Integrated Environment for Developing.. - Tokunaga Takenobu Inui (Correct)
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cl.aist-nara.ac.jp/lab/events/SNLR/papers/12.ps.gz

KUMANO, Tadashi TOKUNAGA, Takenobu INUI, Kentaro TANAKA, Hozumi - Tr- October (Correct)
A realization statement is a syntactic **(structural) constraint** upon the corresponding language grammar problems editing grammar Figure 1: The **flow** of the grammar development tion of the
ftp.cs.titech.ac.jp/pub/TR/94/TR94-0028.ps.gz

Sparc-V9 Architecture Specification With Rapide - Santoro, Park, Luckham (1995) (Correct)
:47 4.3.3 Example 3: **Structural Constraint** :48
components. 4.3.3 Example 3: **Structural Constraint**.**Structural constraints** are a little bit harder to such as if and case statements to help describe the **flow** of information. One could also describe the model
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